Amendments to the Specification:

Please replace the paragraph at page 2, lines 25-28 with the following amended paragraph:

Referring to FIG. 3, the portion of the oxide layer 20 on the semiconductor substrate 10 between the external spacers 22 is removed. The first gate polyoxide layer 19 on the semiconductor substrate 10 between the external spacers 22 is also removed when the oxide layer 20 is etched, to form a patterned second gate polyoxide layer 19a.

Please replace the paragraph at page 6, lines 19-22 with the following amended paragraph:

Preferably, the gate polyoxide layer prevents the silicon nitride layer from separating from the semiconductor substrate and has a thickness of about 50~100 Å. The gate polyoxide layer is an oxide layer formed at a temperature of about 800~900 °C with the injection of oxygen.

Please replace the paragraph at page 13, line 21 - page 14, line 7 with the following amended paragraph:

With reference to FIG. 14, in order to form a self-aligned contact, i.e., an area in which a pad will be formed, a photoresist pattern (not shown) is formed using photolithography to define an area in which a pad will be formed. The first interlevel dielectric layer 116 is etched using the photoresist pattern as an etching mask to form an area in which a pad will be formed. Here, it is preferable that a gas having an etch selectivity ratio of at least 10 of the first interlevel dielectric layer 116 to the silicon nitride layer, e.g., an etch selectivity ratio of about 15 of the first interlevel dielectric layer 116 to the silicon nitride layer, be used as an etching gas. It is preferable that a C-F-based gas such as CF_4, C_5F_8, and C_4F_8 is used as the etching gas. The first interlevel dielectric layer 116 is etched until a silicon nitride layer 110a on the source and drain area 104 is exposed. The oxide layer 112 is removed during the etching process except a portion of the oxide layer 112 protected by an external spacer 114a. In other words, the oxide layer 112a

on the source and drain area 104 [[114]] which is not protected by the external spacer 114a and the oxide layer 112 on the gate electrode 108 is removed during the etching process. The silicon nitride layer 110 on the gate electrode 108 is also removed when the first interlevel dielectric layer 116 is etched. A capping dielectric layer 107 is etched and recessed to a predetermined thickness. The photoresist pattern is removed using a common method, e.g., an ashing process.